PATENT
Customer No. 22,852
Attorney Docket No. 06502.0379-00

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Guy L. STEELE, Jr.	)	Group Art Unit: 2193
	)	
Application No.: 10/035,647	)	Examiner: Mai, Tan V.
	)	
Filed: December 28, 2001	)	
	)	
For: FLOATING POINT DIVIDER WITH EMBEDDED STATUS INFORMATION	)	Confirmation No.: 4097

Mail Stop Appeal Brief--Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF APPEAL BRIEF (37 C.F.R. 41.37)

Transmitted herewith is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on September 30, 2005.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 C.F.R. 41.20(b)(2), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity)

☒ $500.00 (Large Entity)

TOTAL FEE DUE:

Appeal Brief Fee	$ 500.00
Extension Fee (if any)	$1,590.00
Total Fee Due	$2,090.00

☒ Enclosed is a check for $2,090.00 to cover the above fees.

PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this Appeal Brief, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916. A duplicate copy of this paper is enclosed for use in charging the deposit account.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 7, 2006

By: Nathan A. Sloan
Nathan A. Sloan
Reg. No. 56,249

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF UNDER BOARD RULE § 41.37

In support of the Notice of Appeal filed September 30, 2005, and further to Board Rule 41.37, Appellant presents this brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 1.17(c).

This Appeal Brief is being filed concurrently with a Petition for an Extension of Time for four months and the appropriate fee.

This Appeal responds to the Notice of Panel Decision from Pre-Appeal Brief Review mailed on November 8, 2005 and the Final Office Action mailed on June 6, 2005, which rejected claims 1-5 and 7-37 under 35 U.S.C. § 103(a).

04/10/2006 SZEWDIE1 00000018 10035647
02 FC:1254 1590.00 OP

If any additional fees are required or if the enclosed payment is insufficient, Appellant requests that the required fees be charged to Deposit Account No. 06-0916.

04/10/2006 SZEWDIE1 00000018 10035647
01 FC:1402 500.00 OP

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Sun Microsystems, Inc. is the real party in interest, as indicated by the assignment in its name, recorded at Reel 012446, Frame 0682 on December 28, 2001.

II. RELATED APPEALS AND INTERFERENCES

In accordance with 37 C.F.R. § 41.37(c)(1)(ii), Appellant advises the Board of Patent Appeals and Interferences (the "Board") of the following pending appeals, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the instant appeal:

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,595, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,584, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,587, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,579, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,580, in which an Appeal Brief was filed concurrently herewith.

III. STATUS OF CLAIMS

Claims 1-37 remain pending and under current examination.

Claims 1-5 and 7-37 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,995,991 to Huang et al. ("*Huang*"). Appellant appeals this rejection of those claims.

Claims 1-5 and 7-37 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,009,511 to Lynch et al. ("*Lynch*"). Appellant appeals this rejection of those claims.

The attached Appendix contains a clean copy of the claims involved in the appeal, claims 1-37.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendments under 37 C.F.R. § 1.116 have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1, 14, and 26 of this application respectively recite a system, method, and computer-readable medium for providing a floating point division. *Specification*, p. 1, paragraph 002.

Digital electronic devices, such as digital computers, calculators and other devices, perform arithmetic calculations on values in integer, or "fixed point," format, in fractional, or "floating point" format, or both. *Specification*, p. 1, paragraph 003. Institute of Electrical and Electronic Engineers (IEEE) Standard 754, (hereinafter "IEEE Std. 754") published in 1985 and adopted by the American National Standards Institute (ANSI), defines several standard formats for expressing values in floating point format and a number of aspects regarding behavior of computation in connection therewith. *Id.*

In prior art devices that perform floating point computations, floating point status information generated by the computation is stored in a floating point status register. *Id.* at p. 7, paragraph 020. The status information is stored as conditions, represented by flags that are stored in the floating point status register. *Id.* at p. 7, paragraph 026.

However, the modes (*e.g.*, the rounding modes and traps enabled/disabled mode), flags (*e.g.*, flags representing the status information), and traps that are required to implement IEEE Std. 754 introduce implicit serialization issues. *Id.* at p. 8, paragraph 028. Implicit serialization is essentially the need for serial control of access (read/write) to and from globally used registers, such as a floating point status register. *Id.* The potential for implicit serialization makes the Standard difficult to implement coherently and efficiently in today's superscalar and parallel processing architectures without loss of performance. *Id.*

Moreover, the implicit side effects of a procedure that can change the flags or modes can make it very difficult for compilers to perform optimizations on floating point code. *Id.* at pp. 8-9, paragraph 029. As a result, compilers for most languages usually assume that every procedure call is an optimization barrier in order to be safe. *Id.* This unfortunately may lead to further loss of performance. *Id.*

The claimed invention addresses these and other problems of prior art floating point computational systems. *Id.* at p. 9, paragraph 032. Since the floating point status information comprises part of the floating point representation of the result, instead of being separate and apart from the result as in prior art square root units, the implicit serialization that is required by maintaining the floating point status information separate and apart from the result may be obviated. *Id.* at p. 12, paragraph 045.

The invention, as recited by independent claim 1, relates to a system for providing a floating point division (FIG. 1). *Id.* at p. 9, paragraph 034. The system may include an analyzer circuit (FIG. 1, 11A, 11B, 12A, 12B) configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively. *Id.* at pp. 17-18, paragraph 062. The system may also include a results circuit (FIG. 1, 13, 14, 15) coupled to the analyzer circuit and configured to assert a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand and a resulting status embedded within the resulting floating point operand. *Id.*

The invention, as recited by claim 15, relates to a method for providing a floating point division. *Id.* at p. 10, paragraph 035. The method may include determining, using a divider unit (FIG. 10, 10), a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively. *Id.* The method may also include asserting a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand and a resulting status embedded within the resulting floating point operand. *Id.*

The invention, as recited by claim 27, relates to a computer-readable medium on which is stored a set of instructions for providing a floating point division, which when executed perform stages. *Id.* at p. 10, paragraph 036. The stages may include determining a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand

and data within the second floating point operand respectively. *Id.* The stages may also include asserting a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand and a resulting status embedded within the resulting floating point operand. *Id.*

VI. GROUNDS OF REJECTION TO BE REVIEWED

Claims 1-5 and 7-37 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,995,991 to Huang et al. ("*Huang*"). Appellant appeals this rejection of those claims.

Claims 1-5 and 7-37 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,009,511 to Lynch et al. ("*Lynch*"). Appellant appeals this rejection of those claims.

VII. ARGUMENT

A. Introduction

In view of the reasoning set forth below, Appellant respectfully requests the Board to reverse the Examiner's rejections. Each ground of rejection is treated under a separate heading. Groups of claims are placed under a subheading, identifying the claim(s) by number.

B. The rejection of claims 1-5 and 7-37 under 35 U.S.C. § 103(a) as being unpatentable over *Huang*

Several basic factual inquires must be made in order to determine the obviousness or non-obviousness of claims of a patent application under 35 U.S.C. § 103. These factual inquiries, set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), require the Examiner to:

(1) Determine the scope and content of the prior art;
(2) Ascertain the differences between the prior art and the claims in issue;
(3) Resolve the level of ordinary skill in the pertinent art; and
(4) Evaluate evidence of secondary considerations.

The obviousness or nonobviousness of the claimed invention is then evaluated in view of the results of these inquiries. *Graham*, 383 U.S. at 17-18, 148 USPQ 467.

Thus, in order to carry the initial burden of establishing a *prima facie* case of obviousness that satisfies the *Graham* standard, the Examiner must show that the prior art reference teaches or suggests all the claim elements. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The Examiner must also show that there is some suggestion or motivation, either in the reference or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). "Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 1998) (citations omitted). In addition, the suggestion or motivation "must be found in the prior art reference, not in the Appellant's disclosure." *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

1. Claims 1-5 and 7-37 patentably distinguish from *Huang*

Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example, "an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first

floating point operand and data within the second floating point operand respectively," (emphasis added).

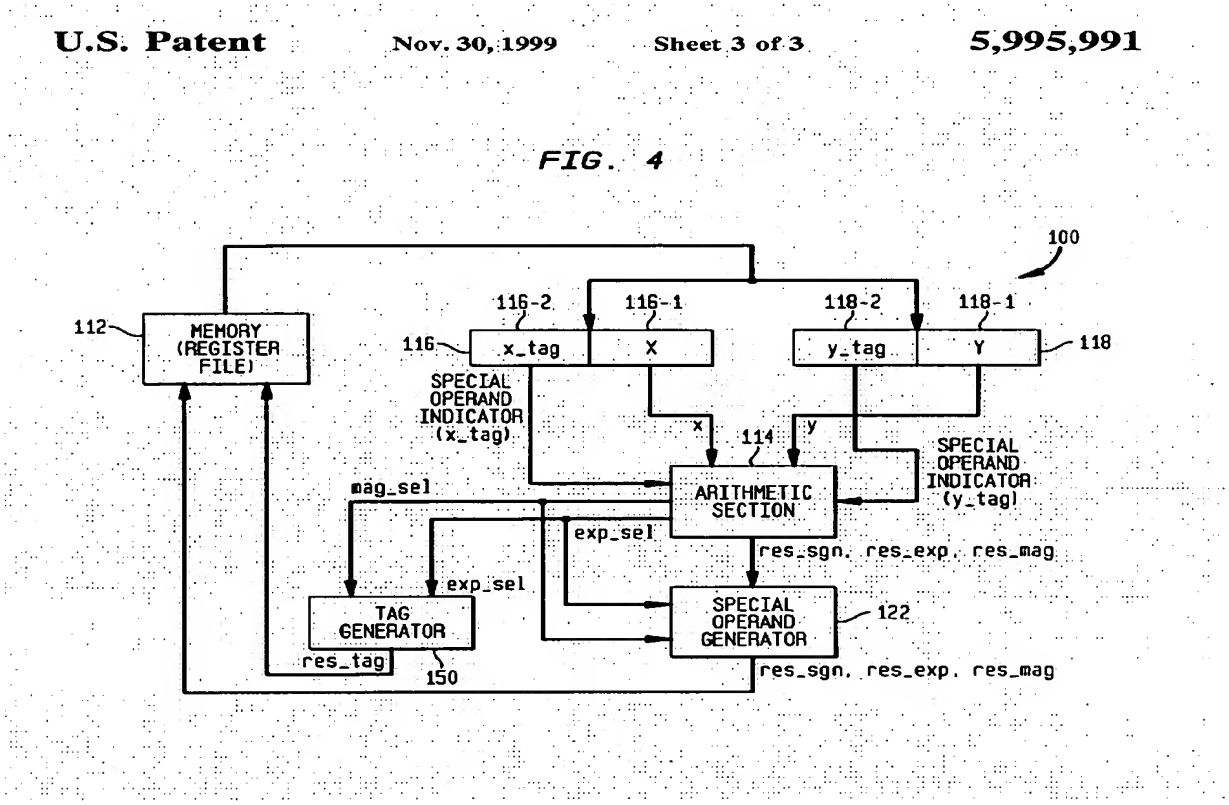
The Examiner concedes that *Huang* fails to teach or suggest this element, stating "Huang et al. do not specifically detail the claimed 'analyzer circuit configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand," (emphasis in original, *Office Action mailed October 12, 2004* at p. 3). Although the Examiner attempts to cure this deficiency of *Huang* by asserting "[h]owever, Huang et al do disclose X and Y operand registers each includes [sic] a special operand indicator" (emphasis added, *Office Action mailed October 12, 2004* at p. 3), the Examiner's assertion fails to cure the deficiencies of *Huang*.

First, the Examiner has not identified specific teachings in *Huang* which show the Examiner's coined term "special operand indicator." The Examiner has also not explained how the coined term relates to, for example, the claimed "determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively," as recited by claim 1 (emphasis added).

Second, even assuming the Examiner's coined term "special operand indicator" refers to a tag value of *Huang* (*Huang*, FIG. 4, 116-2), *Huang's* teaching of a "tag value" does not constitute a teaching or suggestion of "data within the first floating point operand and data within the second floating point operand" (emphasis added) as recited by claim 1.

Huang specifically contradicts that a "tag value" can constitute "data within the ... operand," as recited by claim 1. As illustrated in Fig. 4 of *Huang*, which Appellant

reproduces below, *Huang* teaches "each portion of the registers 116 and 118 has an operand value storage portion 116-1 and 118-1 and a tag value storage portion 116-2 and 118-2" (emphasis added, *Huang*, col. 6, line 66 through col. 7, line 2).



Huang thus teaches a separate operand value storage portion, 116-1, and a separate tag value storage portion for the x_tag 116-2 (*Huang*, col. 6, line 66 through col. 7, line 2; Fig. 4). *Huang's* tag value stored in 116-2 is clearly not "data within" *Huang's* operand value stored in 116-1. Neither this portion of *Huang* nor any other portion can constitute a teaching of an analyzer circuit configured to "determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand," as recited by claim 1 (emphasis added).

Moreover, independent claim 1 recites "a results circuit coupled to the analyzer circuit and configured to ... a resulting status embedded within the resulting floating point operand" (emphasis added). However, the Examiner has not identified any specific teachings of *Huang* which correspond to "a resulting status embedded within the resulting ... operand," as recited by claim 1 (emphasis added). *See Office Action mailed October 12, 2004* at pp. 3-4. Indeed, there are no such teachings. As illustrated in FIG. 4, *Huang* teaches a tag generator 150 to generate the tag (alleged status) separately from the operand, which is loaded separately into tag value portion 116-2 as discussed above. Such teachings by *Huang* do not constitute a teaching or suggestion of "a resulting status embedded within the resulting floating point operand," as recited by claim 1 (emphasis added).

Structures such as those taught by *Huang* were acknowledged in the Background section of Appellant's specification, which states "conditions are typically represented by flags that are stored in the floating point status register" (paragraph 026). Claim 1 specifically distinguishes over such structures, calling for determining a first and second status of a first and second operand "based upon data within the first floating point operand and data within the second floating point operand" (emphasis added). Claim 1 also distinguishes over such structures by calling for "a resulting status embedded within the resulting floating point operand" (emphasis added).

Accordingly, *Huang* does not teach or suggest each and every element recited by claim 1.

Moreover, there is no motivation or suggestion to modify *Huang* to arrive at Appellant's claimed invention. The Examiner relies on a single reference, *Huang*, in

rejecting claims 1-5 and 7-37. Even where the Examiner relies on a single reference, there still "must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 1998) (citations omitted).

The Examiner asserts that it "would have been obvious ... to design the claimed invention according to Huang et al's teachings because the device is an **arithmetic calculation circuit (100)** having special operand indicator in each operand register as claimed." *Office Action mailed October 12, 2004* at p. 3 (emphasis in original). This assertion by the Examiner fails to meet the requisite high threshold of an objective indication that one of skill in the art would modify *Huang* to arrive at Appellant's claimed invention. Merely asserting that a device is an "arithmetic calculation unit" does not constitute motivation to modify *Huang* to arrive at Appellant's claimed invention at least because the Examiner's alleged motivation does not constitute motivation to arrive at Appellant's claimed invention, and the Examiner's alleged motivation is impermissible hindsight.

First, the Examiner's alleged motivation is directed to a special operand indicator "in each operand register." *Id.* (emphasis added). Discussion of "a special operand indicator in each operand register," however, does not constitute motivation to determine a first and second status of a first and second operand "based upon data within the first floating point operand and data within the second floating point operand," as recited by claim 1 (emphasis added). Discussion of "a special operand indicator in each operand register," also does not constitute motivation for "a resulting status

embedded within the resulting floating point operand," as recited by claim 1 (emphasis added).

Second, the Examiner uses impermissible hindsight in reconstructing Appellant's claimed invention. A determination of obviousness must "take into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and ... [must] not include knowledge gleaned only from" Appellant's disclosure. *In re McLaughlin*, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971) (emphasis added). As discussed above, the Examiner concedes that *Huang* does not teach determining a "first status of a first floating point operand and a second status of a second floating point operand." *Office Action mailed October 12, 2004* at p. 3. No other reference is cited to cure this deficiency. Therefore, the Examiner's determination of obviousness could not have been founded on knowledge within the level of skill in the art when Appellant's claimed invention was made. Such determination instead impermissibly relied on hindsight reasoning by looking to Appellant's specification. For at least this additional reason, there is no motivation to modify *Huang* to arrive at Appellant's invention as recited by claim 1.

Accordingly, there is neither a teaching or suggestion of each and every claim element, nor motivation to modify *Huang* to arrive at Appellant's invention recited by claim 1. Therefore, no *prima facia* case of obviousness has been established for claim 1.

Independent claims 14 and 26, although of different scope, recite elements similar to those recited by claim 1. Claims 2-5, 7-13, 15-25, and 27-37 depend from independent claims 1, 14, and 26 and therefore include all of the elements recited

therein. Accordingly, no *prima facie* case of obviousness has been established with respect to claims 2-5 and 7-37 for at least the reasons discussed above regarding claim 1. Appellant requests the Board to overturn the rejection of claims 1-5 and 7-37.

2. Claims 2-5, 7-13, 15-25, and 27-37 patentably distinguish from *Huang*

Huang does not disclose each and every element of dependent claims 2-5, 7-13, 15-25, and 27-37. In fact, the Examiner has not addressed any of the elements recited by dependent claims 2-5, 7-13, 15-25, and 27-37, other than to say that *Huang* "should have" the claimed elements, *Huang* allegedly teaches an "equivalent feature," the claimed elements are "well known," *Huang* is "capable of" the claimed elements, and the claimed elements are "obvious design choice." *See Office Action mailed October 12, 2004* at p. 4. These bare assertions fail to meet the requirement for showing how *Huang* allegedly teaches or suggests each and every element of claims 2-5, 7-13, 15-25, and 27-37. Moreover, the Examiner has not provided any motivation to make the alleged modifications. *Id.*

Because the Examiner has neither shown how the prior art allegedly teaches or suggests each and every claim element, nor shown the requisite motivation to modify *Huang* to arrive at Appellant's claimed invention, no *prima facie* case of obviousness has been established with respect to claims 2-5, 7-13, 15-25, and 27-37. Appellant requests that the Board allow these claims.

C. The rejection of claims 1-5 and 7-37 under 35 U.S.C. § 103(a) as being unpatentable over *Lynch*

1. Claims 1-5 and 7-37 patentably distinguish from *Lynch*

The Examiner's rejections contain clear errors and omit essential elements necessary to establish a *prima facie* case of obviousness for Appellant's claims 1-37 based on *Lynch*.

Independent claim 1 recites a combination including, for example,

> an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

(emphasis added).

The Examiner concedes that *Lynch* fails to teach or suggest this element, stating "Lynch et al. do not specifically detail the claimed 'analyzer circuit configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand'" *Office Action mailed October 12, 2004* at p. 5 (emphasis in original). Moreover, the Examiner has not cited any additional reference to cure this admitted deficiency of *Lynch*, despite Appellant's requests. *See Amendment filed December 16, 2004* at pp. 16-17; *Request for Reconsideration filed August 4, 2005* at p. 9-11.

Instead, the Examiner attempts to cure the deficiency by asserting "[h]owever, Lynch et al do disclose the ... appending tag values to each floating point number, the floating point unit can quickly determine which floating point numbers are special floating point numbers and the type of special floating point number." *Office Action mailed June 6, 2005* at p. 3. The Examiner appears to assert that *Lynch's* element 84

(Fig. 4) constitutes an "operand" which contains tag field 89 (alleged status). *See Office Action mailed October 122, 2004* at p. 5. This is not correct.

In addition, the Examiner has not explained how *Lynch's* "tag values" relate to, for example, determining a "first status ... based upon data within the ... operand," as recited by claim 1. Even if *Lynch's* tag value were to constitute the claimed "status," (which Appellant does not concede) the tag value of *Lynch* is not "data within the ... operand," as recited by claim 1.

Fig. 4 of *Lynch*, which Appellant reproduces below, clearly illustrates that Tag Field 89 (alleged status) and Reg Field 87 (operand) are separate from each other and are stored within register stack 84.

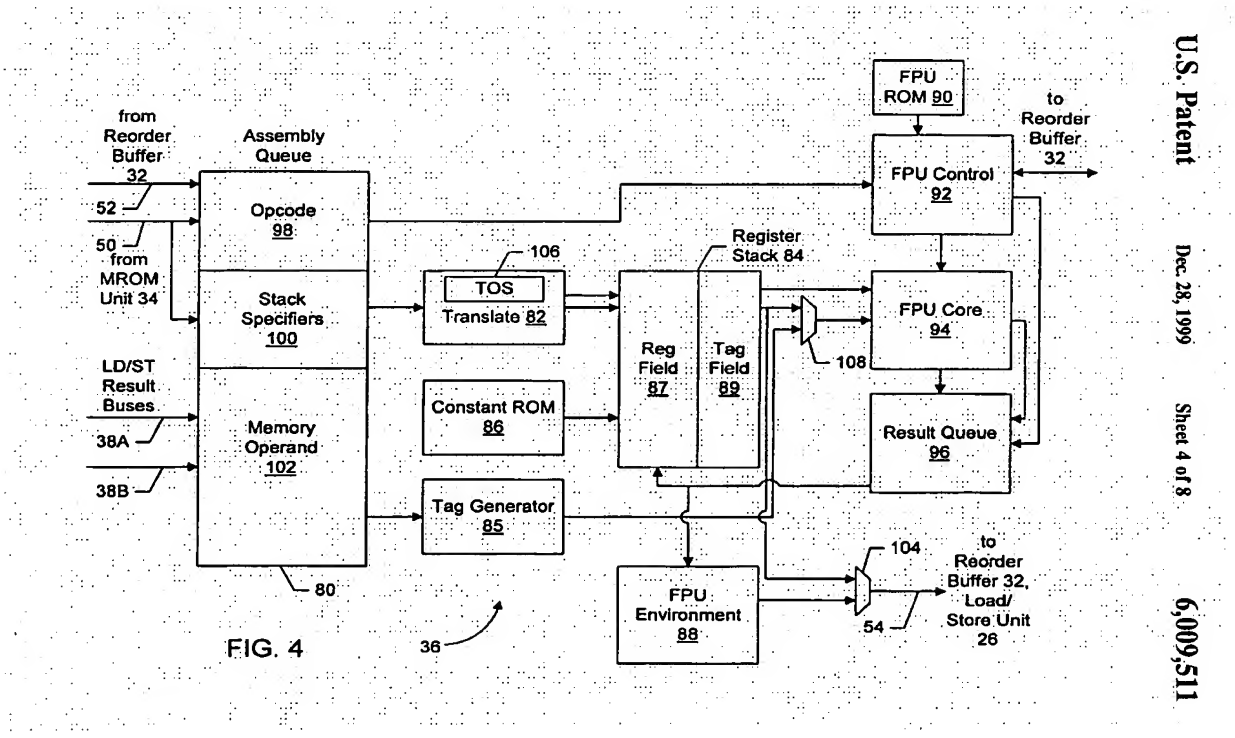


FIG. 4

Moreover, *Lynch* specifically states that element 84 is a register stack, not an operand. *Lynch*, col. 14, lines 47-48. *Lynch* also states that register stack 84 contains a Reg Field 87 for storing an operand separate from a Tag Field 89 for storing a tag

(alleged status). *See Lynch*, col. 15, lines 63-67. "Separate from" cannot constitute "data within" the operand, as recited by claim 1.

In addition, independent claim 1 recites a combination including, for example, "a results circuit coupled to the analyzer circuit and configured to ... a resulting status embedded within the resulting floating point operand" (emphasis added). However, the Examiner has not identified any specific teachings of *Lynch* which would allegedly teach or suggest "a resulting status embedded within the resulting ... operand," as recited by independent claim 1. In fact, the Examiner has not addressed this element at all. *See Office Action mailed October 12, 2004* at pp. 5. This is not surprising, since *Lynch* does not contain a teaching or suggestion of this element. Rather, as discussed above, *Lynch* teaches that the tag value (alleged status) in Tag Field 89 is separate from an operand Reg Field 87. *Lynch* teaches that "[a] tag value is appended to each floating point number stored in a floating point register" (*Lynch*, col. 5, lines 44-45 (emphasis added)), the opposite of the claimed "resulting status embedded within the resulting ... operand."

As with the structures of *Huang*, discussed above, structures such as those taught by *Lynch* were acknowledged in the Background section of Appellant's specification, which states "conditions are typically represented by flags that are stored in the floating point status register" (paragraph 026). Claim 1 specifically distinguishes over such structures, calling for determining a first and second status of a first and second operand "based upon data within the first floating point operand and data within the second floating point operand" (emphasis added). Claim 1 also distinguishes over

such structures by calling for "a resulting status embedded within the resulting floating point operand" (emphasis added).

Because the *Lynch* does not teach or suggest each and every element recited by claim 1, no *prima facie* case of obviousness has been established with respect to claim 1.

Further, there is no motivation or suggestion to modify *Lynch* to arrive at Appellant's claimed invention. As noted above, even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.

Instead of pointing to portions of the cited reference to support the required motivation, the Examiner merely asserts that "it would have been obvious to ... design the claimed invention according to Lynch et al's teachings because the device is a **floating point unit (36)** having the 'determine which floating point numbers are special floating point numbers and the type of special floating point number' as claimed" (*Office Action mailed September 22, 2004* at p. 6, emphasis in original). This assertion by the Examiner fails to meet the requisite high threshold of an objective indication that one of skill in the art would modify *Lynch* to arrive at Appellant's claimed invention. Merely asserting that a device is a "floating point unit" does not constitute motivation to modify *Lynch* to arrive at Appellant's claimed invention at least because the Examiner's alleged motivation does not constitute motivation to arrive at Appellant's claimed invention, and the Examiner's alleged motivation is impermissible hindsight.

In this regard, the Examiner discusses determining "which floating point numbers are special floating point numbers and the type of special floating point number" (*Office*

Action mailed September 22, 2004 at p. 6). However, such discussion of generally determining "which numbers are special floating point numbers" also cannot constitute motivation to determine a first and second status of a first and second operand "based upon data within the first floating point operand and data within the second floating point operand," as recited by claim 1 (emphasis added). The discussion of generally determining "which numbers are special floating point numbers" also does not constitute motivation for modifying *Lynch* to employ "a resulting status embedded within the resulting floating point operand," as recited by claim 1 (emphasis added).

Moreover, *Lynch* teaches "a tag value is appended to each floating point number stored in a floating point register" (*Lynch*, col. 5, lines 44-45). This is the opposite of the claimed structure, which requires "a resulting status embedded within the resulting floating point operand" (emphasis added).

Finally, the Examiner again uses impermissible hindsight in reconstructing Appellant's claimed invention. As discussed above, the Examiner concedes that *Lynch* does not teach "a first status of a first floating point operand." *Office Action mailed October 12, 2004* at p. 5. No other reference is cited to cure this deficiency. Therefore, the Examiner's determination of obviousness could not have been founded on knowledge within the level of skill in the art when Appellant's claimed invention was made. Such determination instead impermissibly relied on hindsight reasoning by looking to Appellant's specification. For at least this additional reason, there is no motivation to modify *Lynch* to arrive at Appellant's invention as recited by claim 1.

Because *Lynch* contains neither a teaching or each and every element of claim 1, nor has the Examiner shown the requisite motivation to modify *Lynch* to arrive at

Appellant's invention recited by claim 1, no *prima facia* case of obviousness has been established.

Independent claims 14 and 26, although of different scope, recite elements similar to those recited by claim 1. Claims 2-5, 7-13, 15-25, and 27-37 depend from independent claims 1, 14, and 26 and therefore include all of the elements recited therein. Accordingly, no *prima facie* case of obviousness has been established with respect to claims 2-5 and 7-37 for at least the reasons discussed above regarding claim 1. Appellant requests the board to allow claims 1-5 and 7-37.

2. Claims 2-5, 7-13, 15-25, and 27-37 patentably distinguish from *Lynch*

Lynch does not disclose each and every element of dependent claims 2-5, 7-13, 15-25, and 27-37. In fact, the Examiner has not addressed any of the elements recited by dependent claims 2-5, 7-13, 15-25, and 27-37, other than to say that *Lynch* "should have" the claimed elements, *Lynch* allegedly teaches an "equivalent feature," the claimed elements are "well known," *Lynch* is "capable of" the claimed elements, and the claimed elements are "obvious design choice." *See Office Action mailed October 12, 2004* at p. 5-6. These unsupported assertions also fail to meet the requirement for a teaching or suggestion in *Lynch* of each and every element of claims 2-5, 7-13, 15-25, and 27-37. The Examiner also has not shown the required motivation to modify *Lynch* to achieve the claimed combination. *Id.*

Because the Examiner has shown neither a teaching or suggestion in the prior art of each and every claim element, nor the requisite motivation to modify the prior art to arrive at Appellant's claimed invention, no *prima facie* case of obviousness has been

established with respect to claims 2-5, 7-13, 15-25, and 27-37. Appellant requests that the Board allow these claims.

D. Summary

The Examiner has not established a *prima facie* case of obviousness with respect to the presently appealed claims. In particular, the references cited by the Examiner in the appealed rejections do not teach or suggest all of the claim limitations. Furthermore, there is no suggestion or motivation, either in the cited references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine references, and the references, in fact, teach away from the claimed structure. *See* M.P.E.P. § 2143. Thus, the Examiner has failed to meet the criteria required for a *prima facie* showing of obviousness.

VIII. CONCLUSION

For the reasons given above, pending claims 1-37 are allowable and reversal of the Examiner's rejections are respectfully requested.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 7, 2006

By: _____
Nathan A. Sloan
Reg. No. 56,249

IX. Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

1. A system for providing a floating point division, comprising:

an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

a results circuit coupled to the analyzer circuit and configured to assert a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand and a resulting status embedded within the resulting floating point operand.

2. The system for providing a floating point division of claim 1, wherein the analyzer circuit further comprises:

a first operand buffer configured to store the first floating point operand;

a second operand buffer configured to store the second floating point operand;

a first operand analysis circuit coupled to the first operand buffer, the first operand analysis circuit configured to generate a first characteristic signal having information relating to the first status; and

a second operand analysis circuit coupled to the second operand buffer, the second operand analysis circuit configured to generate a second characteristic signal having information relating to the second status.

3. The system for providing a floating point division of claim 2, wherein the first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer.

4. The system for providing a floating point division of claim 3, wherein the memory storage external to the first operand buffer and the second operand buffer is a floating point status register.

5. The system for providing a floating point division of claim 1, wherein the results circuit further comprises:

a divider circuit coupled to the analyzer circuit, the divider circuit configured to produce the result of the division of the first floating point operand by the second floating point operand;

a divider logic circuit coupled to the analyzer circuit and configured to produce the resulting status based upon the first status and the second status; and

a result assembler coupled to the divider circuit and the divider logic circuit, the result assembler configured to assert the resulting floating point operand and embed the resulting status within the resulting floating point operand.

6. The system for providing a floating point division of claim 5, wherein the divider logic circuit is organized according to the structure of a decision table.

7. The system for providing a floating point division of claim 1, wherein the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, a division by zero status, an infinity status, and an inexact status.

8. The system for providing a floating point division of claim 7, wherein the overflow status represents one in a group of a +ON status and a -ON status.

9. The system for providing a floating point division of claim 8, wherein the overflow status is represented as a predetermined non-infinity numerical value.

10. The system for providing a floating point division of claim 7, wherein the underflow status represents one in a group of a +UN status and a -UN status.

11. The system for providing a floating point divider of claim 10, wherein the underflow status is represented as a predetermined non-zero numerical value.

12. The system for providing a floating point division of claim 7, wherein the invalid status represents a not-a-number (NaN) status due to an invalid operation.

13. The system for providing a floating point division of claim 7, wherein the infinity status represents one in a group of a positive infinity status and a negative infinity status.

14. A method for providing a floating point division, comprising:

determining, using a divider unit, a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

asserting a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand and a resulting status embedded within the resulting floating point operand.

15. The method for providing a floating point division of claim 14, wherein the determining stage further comprises:

storing the first floating point operand in a first operand buffer;

storing the second floating point operand in a second operand buffer;

generating a first characteristic signal representative of the first status; and

generating a second characteristic signal representative of the second status.

16. The method for providing a floating point division of claim 15, wherein the first characteristic signal and the second characteristic signal are generated without regard to memory storage external to the first operand buffer and the second operand buffer.

17. The method for providing a floating point division of claim 16, wherein the memory storage external to the first operand buffer and the second operand buffer is a floating point status register.

18. The method for providing a floating point division of claim 14, wherein the asserting stage further comprises:

producing the result of the division of the first floating point operand by the second floating point operand; and

asserting the resulting floating point operand having the resulting status embedded within the resulting floating point operand.

19. The method for providing a floating point division of claim 14, wherein the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, a division by zero status, an infinity status, and an inexact status.

20. The method for providing a floating point division of claim 19, wherein the overflow status represents one in a group of a +OV status and a -OV status.

21. The method for providing a floating point division of claim 20, wherein the overflow status is represented as a predetermined non-infinity numerical value.

22. The method for providing a floating point division of claim 19, wherein the underflow status represents one in a group of a +UN status and a -UN status.

23. The method for providing a floating point division of claim 22, wherein the underflow status is represented as a predetermined non-zero numerical value.

24. The method for providing a floating point division of claim 19, wherein the invalid status represents a not-a-number (NaN) status due to an invalid operation.

25. The method for providing a floating point division of claim 19, wherein the infinity status represents one in a group of a positive infinity status and a negative infinity status.

26. A computer-readable medium on which is stored a set of instructions for providing a floating point division, which when executed perform stages comprising:

determining a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

asserting a resulting floating point operand containing the result of the division of the first floating point operand by the second floating point operand and a resulting status embedded within the resulting floating point operand.

27. The computer-readable medium of claim 26, wherein the determining stage further comprises:

storing the first floating point operand in a first operand buffer;

storing the second floating point operand in a second operand buffer;

generating a first characteristic signal representative of the first status; and

generating a second characteristic signal representative of the second status.

28. The computer-readable medium of claim 27, wherein the first characteristic signal and the second characteristic signal are generated without regard to memory storage external to the first operand buffer and the second operand buffer.

29. The computer-readable medium of claim 28, wherein the memory storage external to the first operand buffer and the second operand buffer is a floating point status register.

30. The computer-readable medium of claim 26, wherein the asserting stage further comprises:

producing the result of the division of the first floating point operand by the second floating point operand; and

asserting the resulting floating point operand having the resulting status embedded within the resulting floating point operand.

31. The computer-readable medium of claim 26, wherein the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, a division by zero status, an infinity status, and an inexact status.

32. The computer-readable medium of claim 31, wherein the overflow status represents one in a group of a +OV status and a -OV status.

33. The computer-readable medium of claim 32, wherein the overflow status is represented as a predetermined non-infinity numerical value.

34. The computer-readable medium of claim 31, wherein the underflow status represents one in a group of a +UN status and a -UN status.

35. The computer-readable medium of claim 34, wherein the underflow status is represented as a predetermined non-zero numerical value.

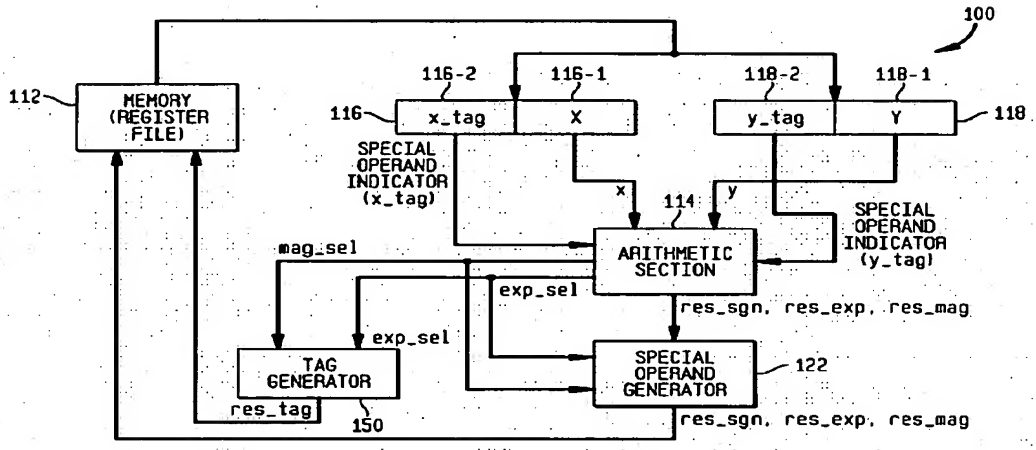
36. The computer-readable medium of claim 31, wherein the invalid status represents a not-a-number (NaN) status due to an invalid operation.

37. The computer-readable medium of claim 31, wherein the infinity status represents one in a group of a positive infinity status and a negative infinity status.

X. Evidence Appendix to Appeal Brief Under Rule 41.37(c)(1)(ix)

Appellant relies on Fig. 4 of *Huang* and Fig. 4 of *Lynch*, both of which are reproduced below.

FIG. 4



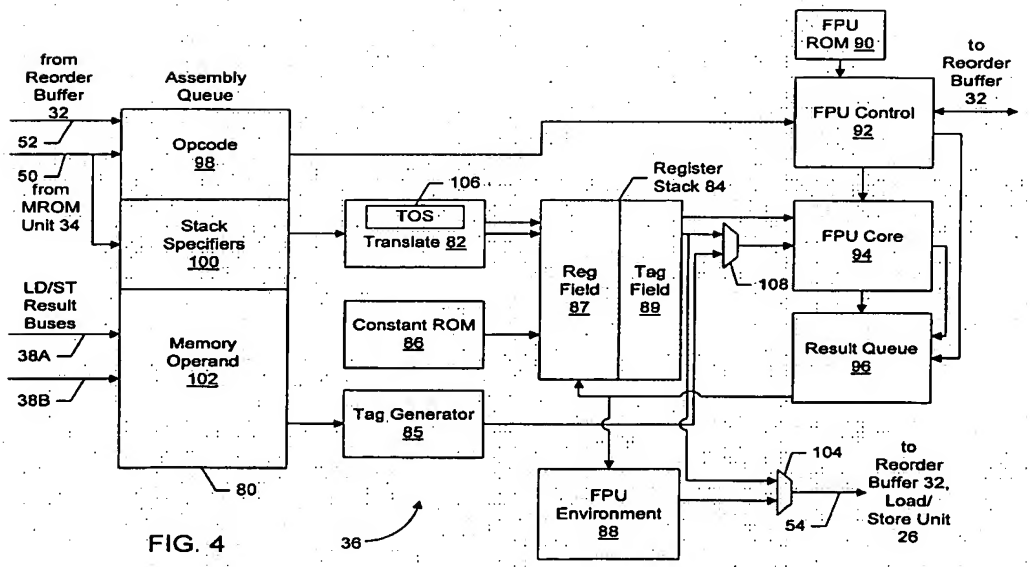


FIG. 4

XI. Related Proceedings Appendix to Appeal Brief Under Rule 41.37(c)(1)(x)

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,595, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,584, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,587, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,579, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,580, in which an Appeal Brief was filed on concurrently herewith.